Three-Dimensional Silicon MMIC's Operating up to *K*-Band

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***Abstract*— This paper presents three-dimensional (3-D) Si monolithic microwave integrated circuit (MMIC) technology and Si MMIC operation up to K-band using this technology, and describes X- and K-band mixers with design details and measurements. The 3-D Si MMIC technology isolates passive circuits from the low-resistivity Si substrate. The evaluations use Si bipolar transistors with an emitter size of 0.3 μm × 13.4 μm × 9 and $f_{\max}$ of 30 GHz. The mixers are base and collector LO injection types. The mixers, fabricated in an area of 0.76 mm × 0.54 mm for the X-band mixers and in 0.46 mm × 0.42 mm for the K-band mixers, exhibit a frequency conversion loss of 5–12 dB from 3.5 to 10 GHz and from 10 to 25 GHz. This technology is extremely effective for single-chip integration of receivers and transmitters and also for mixed-mode MMIC's up to K-band frequencies.**

***Index Terms*—Bipolar transistor, masterslice, mixer, MMIC's, multilayer, silicon, three-dimensional structure.**

I. Introduction

WIRELESS communication systems such as mobile, satellite, and wireless local area networks (LAN's), will require high-frequency operation and low fabrication cost to support truly effective multimedia services. This will require advances in the equipment used in these systems. Silicon-based microwave integrated circuits (IC's) are suitable for these applications because they have a low fabrication cost due to the use of the digital IC process and because they can achieve highly integrated multifunctional IC's such as analog–digital mixed IC's. Conventional Si microwave monolithic integrated circuits (MMIC's) [1]–[4] which consist of circuits elements such as differential pair transistors, Gilbert cells, or on-chip inductors that combine them, can not achieve X-band operation frequencies, even if high-performance Si devices are used. The low resistivity of the silicon wafer obstructs the reactive impedance matching design needed for higher frequency operation. To overcome the above problems, several approaches have been reported to suppress the transmission loss, such as by using a high-resistivity ($>$1 k$\Omega\cdot$cm) Si substrate [5]–[7], thick dielectric film as an insulator [8], [9], stacked multilevel conductors [10], the silicon-on-insulator (SOI) technology [11], [12], or employing a coplanar structure on the Si substrate [5]–[7], [13]. However, these methodologies neither offer sufficient performance in the K-band, nor do they offer a compact circuit area for highly integrated MMIC's, even though the MMIC's employ state-of-the-art high-performance transistors.

Three-dimensional (3-D) masterslice MMIC technology [14]–[17] is very effective in solving the above problems. The remarkable advantages of this technology are:

1) miniature and accurate distributed-line-type passive circuits can be constructed over a ground metal on the surface of an Si wafer;
2) ground metal separates the Si wafer from the passive circuit components;
3) Q factor of the thin-film transmission lines is as high as 17 at 20 GHz; and
4) structure is compatible with gate-array-type fabrication.

This paper presents 3-D masterslice Si MMIC's for K-band operation. First, the 3-D masterslice MMIC structure, which is compatible with gate-array-type fabrication and its features, are described. Second, X- and K-band mixers, which are among the most important RF circuits, are designed and demonstrated. These mixers operate at low supply voltages because mixing is based on collector current nonlinearity. Third, the measured and predicted performance levels of 3-D Si MMIC amplifiers are evaluated. Finally, additional discussions will address the single-chip integration of receivers, transmitters, transceivers, and for mixed-mode Si MMIC's for K-band operation.

II. 3-D Masterslice Si MMIC Structure

A. Structure

Fig. 1 shows the basic structure of the 3-D masterslice Si MMIC. Transistors, resistors, lower metals (first-level metals) for metal-insulator-metal (MIM) capacitors, the passivation layer, and second-level metals ($GND1$, shown in Fig. 1) are formed on an Si substrate using the standard Si IC process. The first- and second-level metals are aluminum. The 3-D passive structure, consisting of four layers of 2.5-μm-thick polyimide film and four layers of 1-μm-thick gold conductor metal (top-level metal is 2-μm-thick) is formed on the top-level metal using the Si IC process. Pads to connect bonding wires or for on-wafer measurements are formed on the top-level metal of the 3-D structure. This position offers greatly

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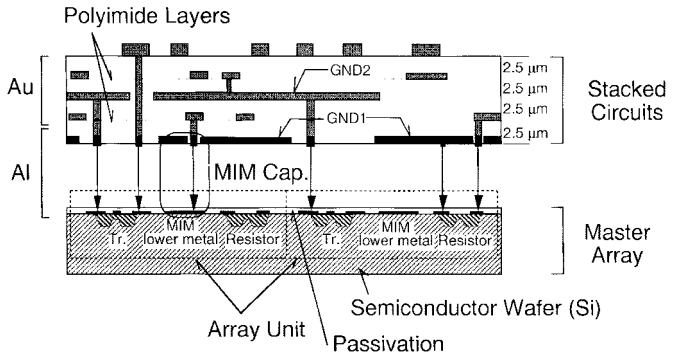


Fig. 1. Basic structure of 3-D masterslice Si MMIC.

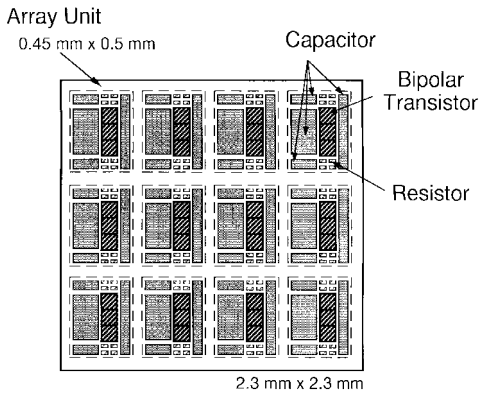


Fig. 2. Master array on Si substrate.

reduced parasitic capacitance. This is because the polyimide has low permittivity. The 3-D structure is fabricated by folded-metal interconnection technology (FMIT) with thick insulator [16]. The fabricated polyimide thickness is within 2% standard deviation over the 3-in-diameter wafer [15], and a high level of reliability of the 3-D structure was guaranteed by temperature-cycle tests and bias stress tests given in [18]. The 3-D structure fabrication process allows a connection between the 3-D passive circuits and the rugged surface wafer due to the use of polyimide films. This results in a wide range of applications such as CMOS, BiCMOS, high electron-mobility transistor (HEMT), and heterojunction bipolar transistor (HBT) devices. Isolation of the passive circuits from the conductive property of the Si substrate is achieved by covering the substrate with $GND1$, resulting in low-loss passive circuits. This means that the reactive matching method, which compensates the parasitic capacitance of the transistors, can be used, which allows Si MMIC's on standard Si wafers to achieve K-band operation.

Fig. 2 shows an example of a master array on a 2.3 mm $\times$ 2.3 mm Si substrate. Twelve array units, each containing transistors, resistors, and the lower metal of MIM capacitors, are placed on a wafer to form the master array. On-wafer elements not selected in a design are covered with $GND1$ and the passive circuits are formed on top of $GND1$. The masterslice MMIC technology is the same as that used with GaAs substrate [14], [15] and realizes the gate-array-type fabrication in the microwave field. This technology achieves a high integration level and effectively reduces the development turnaround time (TAT), resulting in low fabrication cost.

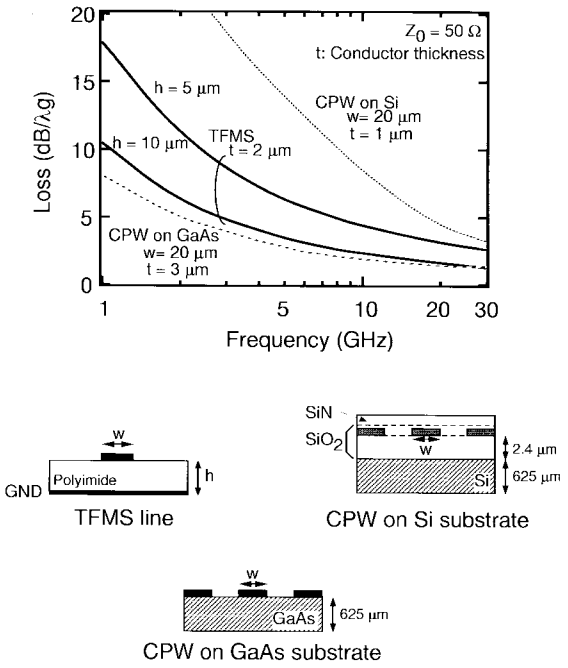


Fig. 3. Comparison between the calculated attenuation of TFMS lines and CPW's.

B. Characteristics of Transmission Lines

Fig. 3 compares the line losses between the thin-film microstrip (TFMS) lines on the 3-D structure and the coplanar waveguide (CPW) on an Si or GaAs substrate. These results were calculated by the full-wave finite-element method (FEM). The thickness of each transmission line is based on the use of practical fabrication processes. In the K-band, losses of the 50-Ω TFMS lines are 50% lower than that of a 50-Ω CPW with a 2.4-μm-thick insulator on a Si substrate with a resistivity of 30 $\Omega\cdot$cm, fabricated using the Si IC process, and are competitive with those of CPW on GaAs substrate. These results also show that the Q factors of the CPW's on an Si substrate and the TFMS line with a 10-μm-thick substrate are less than 7 and more than 17 in the K-band, respectively. The Q factors of the TFMS lines are sufficiently high to permit a reactive matching design in the K-band. This figure indicates that the 3-D masterslice MMIC technology promises millimeter-wave operation of Si-based MMIC's.

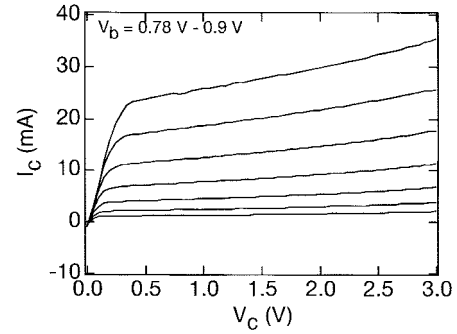
III. X- and K-Band Mixer

A. Device Characteristics

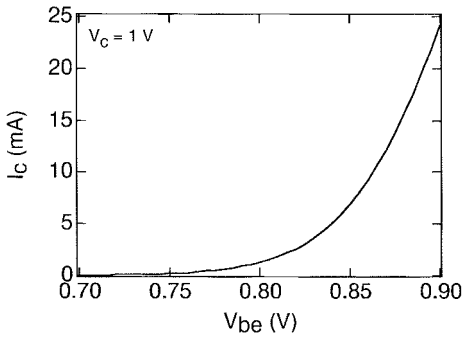
A 0.5-μm Si bipolar transistor process [19] and 3-D masterslice MMIC technology were used for mixer implementation. Transistor size was nine 0.3 μm $\times$ 13.4 μm emitters and its current capacity (36 mA) was comparable to that of a 200-μm gatewidth GaAs MESFET with 0.3-μm gate length. The measured f_T and $f_{\max}$ were 24 GHz and 30 GHz at $V_c = 1$ V, respectively. These values are lower than those of small emitter transistors for digital IC's because of the multiemitter configuration. Other key parameters are shown in Table I, and the *I–V* characteristics of the used transistor are shown in Fig. 4(a) and (b). This figure shows the existence

TABLE I
DEVICE PARAMETERS OF 9 × 0.3 μm × 13.4 μm EMITTER SI BIPOLAR TRANSISTOR. @ $V_{ce} = 1$ V

Emitter area	0.3 μm x 13.4 μm x 9
r_b	5.56 Ω
C_{jeo}	279 fF
C_{jco}	279 fF
C_{jso}	273 fF
f_T , f_{max}	24, 30 GHz
h_{FE}	55
BV_{CEO}(I_c=10mA)	3.6 V
BV_{CBO}	9 V



(a)



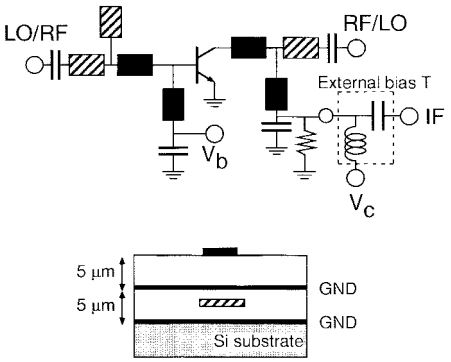
(b)

Fig. 4. *I–V* characteristics of 9 × 0.3 μm × 13.4 μm emitter Si bipolar transistor. (a) I_C–$V_{\rm CE}$ characteristics. (b) I_C–$V_{\rm BE}$ characteristics.

of nonlinearity regions such as a pinchoff region, which support mixing operation, and shows that mixers based on the nonlinearity of transistor parameters operate at very low supply voltages.

B. X-Band Mixer

Mixers were fabricated as common-emitter transistors and reactive matching circuits. A single-transistor active-mixer configuration is selected, and mixing is done by the nonlinearity of the collector current. This means an IF signal is mainly generated by the nonlinearity of the transconductance and the collector–emitter conductance. This mixer configuration also offers a lower supply voltage operation than the Gilbert-cell-type mixer configuration.



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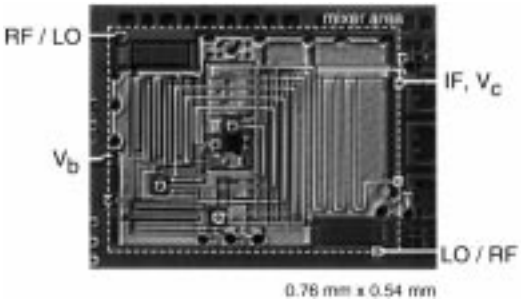


(b)

Fig. 5. Fabricated X-band mixer. (a) Equivalent circuit. (b) Microphotograph.

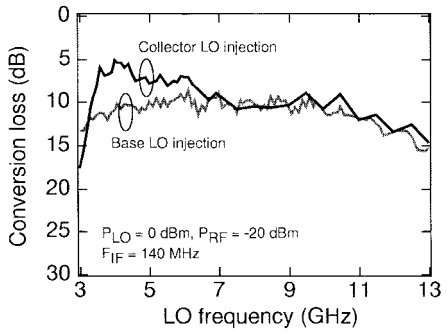
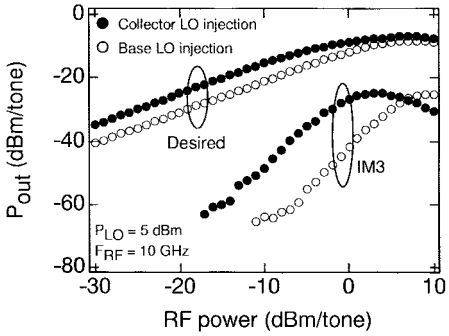


Fig. 6. Measured conversion loss of X-band mixer.

Fig. 5(a) shows the equivalent circuit of an X-band mixer. This mixer offers both base and collector LO injection operation. The generated IF signal emerges from the collector side. Matching circuits constructed with TFMS lines and triplate lines were optimized for RF and LO frequencies, respectively. In addition, the matching circuits are stacked above and below the middle ground plane, which reduces circuit size. Collector bias is supplied via the IF output port with an external bias-T. Fig. 5(b) shows a microphotograph of the X-band mixer. The mixer was fabricated on a master array. The matching circuits are formed in a meander or spiral formation around the transistor, resulting in an area of just 0.76 mm × 0.54 mm. This size is small enough to achieve a single-chip highly integrated MMIC. Fig. 6 shows the conversion loss of the mixer. The black and gray lines plot the conversion loss of the collector and the base LO injection operation, respectively. The conversion loss of collector LO injection operation is 8 dB ±3 dB from 3.5 to 10 GHz, where the LO and RF



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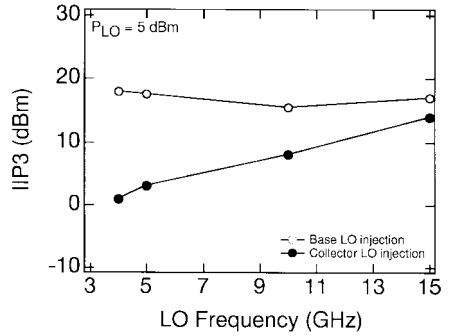


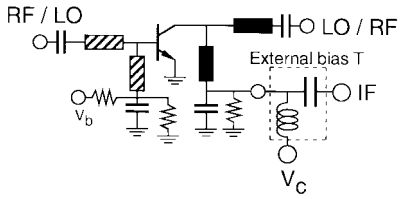
(b)

Fig. 7. Distortion performance of X-band mixer. (a) Measured IM3 performance at 10 GHz. (b) Measured input IP3 performance.

powers are 0 dBm and −20 dBm, respectively. IF frequency is 140 MHz. The collector voltage and base voltage are 0.6 and 0.77 V, respectively, and the power consumption is 1.1 mW. The conversion loss of the base LO injection operation is −10 dB ±1.5 dB from 3.5 to 10 GHz under the same signal conditions as the collector LO injection operation. Collector and base voltages are 0.6 and 0.81 V, respectively, and the power consumption is 3.4 mW. This mixer operates over a very wide-band frequency with low-power-supply voltage and low-power consumption. Fig. 7(a) shows the distortion performance levels of both types of mixer operation. The black circles plot collector LO injection operation and the white circles plot base LO injection operation, where the LO power is 5 dBm and the LO frequency is 10 GHz. When the RF power is −10 dBm, third-order intermodulation (IM3) distortion ratios of the collector and base LO injection operations are 32 and 42 dB, respectively. The input third-order intercept points (IP3) are shown in Fig. 7(b). Input IP3 with base LO injection operation is higher than that with collector LO injection operation and greater than 15 dBm over a very wide-band frequency from 3.5 to 15 GHz. The demonstrated mixers achieve both very wide-band frequency operation and high values of input IP3 despite their very low-power consumption and low-power supply. The differences between them are caused by the collector–emitter conductance and become smaller as the frequency increases.

C. K-Band Mixer

Fig. 8(a) shows the equivalent circuit of a K-band mixer. The mixer configuration is nearly the same as that of the



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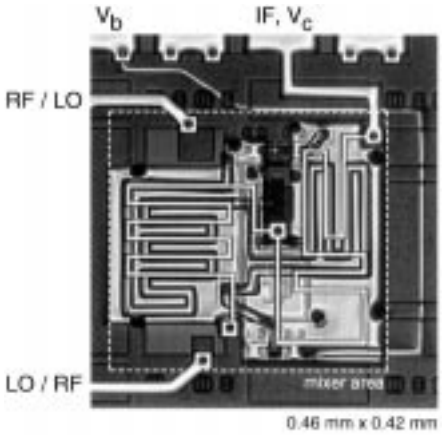


(b)

Fig. 8. Fabricated K-band mixer. (a) Equivalent circuit. (b) Microphotograph.

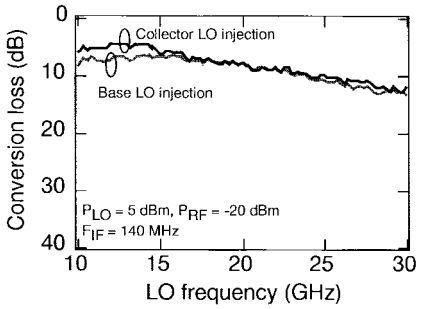
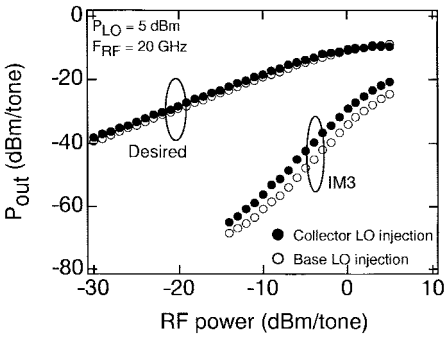


Fig. 9. Measured conversion loss of K-band mixer.

previously presented X-band mixer. The base-side matching circuit uses triplate TFMS lines because the input impedance of the base is very low. The collector-side matching circuit comprises TFMS lines with a 5-μm-thick substrate. The simple matching circuits are possible because of the low-input impedance of the transistor, whose value changes only slightly over the frequency range of 10–30 GHz, resulting in the broad-band performance of the mixer. The matching circuits are stacked above and below the middle ground plane, which ensures compactness. Base bias is supplied via a resistor, and collector bias is supplied via an external bias-T from the IF output port. Fig. 8(b) shows a microphotograph of the K-band mixer. The transmission lines are formed in a meander-like formation, resulting in an area of just 0.46 mm × 0.42 mm. The conversion losses are shown in Fig. 9. The conversion losses are 8 dB ±1 dB from 16.5 to 23 GHz on both types of operation (8.5 dB ±3.5 dB with collector LO injection operation and 10 dB ±2 dB with base LO injection operation from 10 to 30 GHz), where the LO and RF power are 5 dBm and −20 dBm, respectively. The IF frequency is 140 MHz



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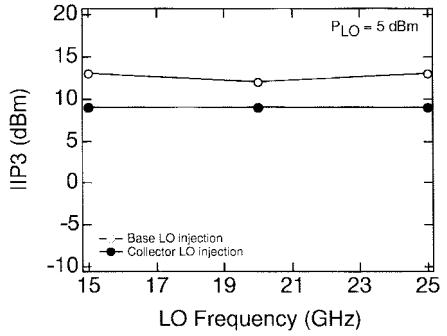


(b)

Fig. 10. Distortion performance of K-band mixer. (a) Measured IM3 performance at 20 GHz. (b) Measured input IP3 performance.

TABLE II
COMPARISON BETWEEN FABRICATED 3-D SI MMIC K-BAND MIXER AND GaAs MESFET MMIC K-BAND MIXER

Device	0.5 μm Si bipolar		0.3 μm GaAs MESFET	
LO injection port	Base	Collector	Drain	Gate
Gain (dB)	-8.5	-7.7	-3.0	-8.5
IP3 (dBm)	12	9	5.6	12.5
Power consumption (mW)	6.99	6.58	0	0
Transistor size(μm)	0.3 x 13.4 x 9		0.3 x 200	
Area (mm^2)	0.46 x 0.42		1.1 x 1.2	
LO power (dBm)	5		10	
Structure	3-D MMIC		Uniplanar MMIC	
	This work		[20]	

and V_c and V_b are 0.3 V and 1.6 V, respectively. The power consumption for both is less than 7 mW. This mixer achieves very wide-band frequency operation despite its simple circuit design and very compact circuit area. Fig. 10(a) shows the distortion performance levels of both types of mixer operation. The black circles plot collector LO injection operation and the white circles plot base LO injection operation; the LO power is 5 dBm and LO frequency is 20 GHz. The IM3 distortion ratios with collector and base LO injection operation are 38 and 42 dB, respectively, when the RF power is −10 dBm. The input IP3's are shown in Fig. 10(b). The IP3 with base LO injection operation is higher than that with collector LO injection operation, approximately 13 dBm over the very wide-band frequency from 15 to 25 GHz. Table II compares the

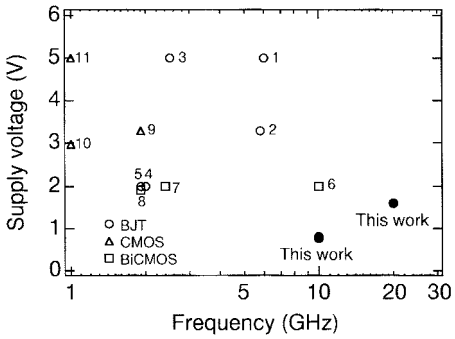


Fig. 11. State-of-the-art supply voltage of Si MMIC mixer up to the 1-GHz frequency range. 1: Gilbert cell [20]. 2: Gilbert cell, on-chip inductor [3]. 3: Gilbert cell [21]. 4: Current folded mixer [22]. 5: Cascode, on-chip inductor [12]. 6: Gilbert cell [23]. 8: Gilbert cell, passive balun [24]. 9: Gilbert cell [25]. 10: Gilbert cell [26]. 11: Differential pair [27].

performance levels of this fabricated K-band mixer to those of a published uniplanar GaAs MESFET mixer MMIC [20] with 200-μm gatewidth. The GaAs MESFET mixer uses the drain LO injection operation and the resistive mixer operation (gate LO injection) with no drain supply voltage, resulting in no power consumption. The gain and the IP3 performance levels of the fabricated Si mixer for the base LO injection operation are comparable to those of the GaAs MESFET resistive mixer. The linearity of the collector LO injection Si bipolar mixer is better than that of the drain LO injection GaAs MESFET mixer. These comparisons indicate that the performance levels of the 3-D MMIC Si bipolar mixer are competitive to those of the GaAs MESFET mixer in the K-band.

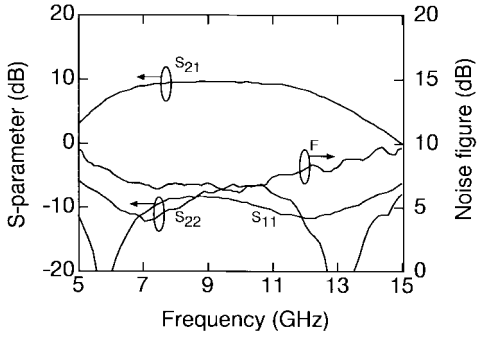
D. State-of-the-Art Mixer Supply Voltage

Fig. 11 shows a supply voltage comparison between recently reported Si MMIC mixers in the microwave frequency range and the mixer introduced in this paper. The reported mixers use Si bipolar, CMOS, or BiCMOS technologies, and are primarily designed on the Gilbert-cell mixer configuration. In this figure, white circles, triangles, and rectangles show Si bipolar, CMOS, and BiCMOS mixers, respectively. The black circles show the X- and K-band fabrication mixers of this paper. The conventional mixers have relatively high supply voltages of around 2 V because the Gilbert-cell mixer configuration uses two or three transistors connected in series. The presented mixers easily achieve the very low supply voltages of around 0.8 V (X-band mixer) and 1.6 V (K-band mixer). The K-band mixer should achieve under 1-V operation if the voltage is supplied without a resistor. In addition, the 3-D MMIC technology shows promise in achieving compact balanced or double-balanced mixers, constructed as unit mixers and very compact 3-D MMIC hybrids, without increasing the supply voltage.

IV. APPLICATION TO HIGHLY INTEGRATED AND MIXED-MODE MMICS

A. Amplifier

The amplifier is also an important circuit for highly integrated multifunction MMIC's. We demonstrate the operation



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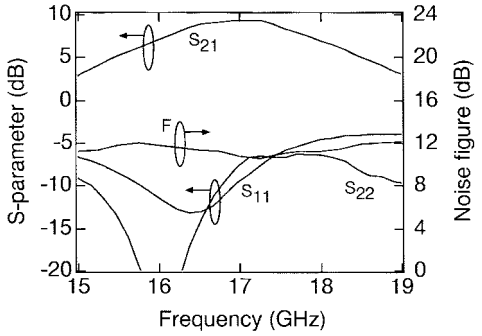


(b)

Fig. 12. Measured performance of 3-D Si MMIC amplifiers. (a) X-band amplifier. (b) K-band amplifier.

of X- and K-band amplifiers employing cascode-connected Si bipolar transistors [15], [17]. The same transistor as used in the presented mixers is employed. The cascode configuration achieves a higher maximum available gain than the single common-emitter transistor, Darlington-pair, or differential-pair configurations, resulting in operation in a higher frequency range. The matching circuits of the X-band amplifier comprise TFMS lines with 5-μm-thick substrate and triplate lines, which are stacked to reduce the circuit area. The matching circuits of the K-band amplifier comprise TFMS lines with a 10-μm-thick substrate to achieve low transmission loss. The circuit areas of the X- and K-band amplifiers are 0.33 mm^2 and 0.3 mm^2, respectively. Fig. 12 shows the measured performance levels of the amplifiers. The X-band amplifier achieves a gain of 8.5 dB $\pm$1 dB, return losses of less than $-$7 dB over a frequency range of 6–12.5 GHz. The noise figure is 6.1 dB at 10 GHz. The K-band amplifier achieves a gain of 8 dB $\pm$1 dB, return losses of less than $-$5 dB over a frequency range of 16–18 GHz. The noise figure is 10 dB at 17 GHz. The supply voltage of both amplifiers is the collector voltage of 4 V. These performance levels are almost the same as those of amplifiers fabricated using GaAs MESFET's. The noise figure will be improved by using low noise matching. Fig. 13 compares conventional Si MMIC amplifiers and fabricated and anticipated 3-D Si MMIC amplifiers. The conventional Si MMIC amplifiers operating in the X-band, shown in Fig. 13, comprise the Darlington pair configuration and use transistors with $f_{\max} = 38$ GHz. The fabricated 3-D Si MMIC amplifiers achieve K-band operation and more than 20-dB gain for three-stage amplification. The black bar shows the simulation result

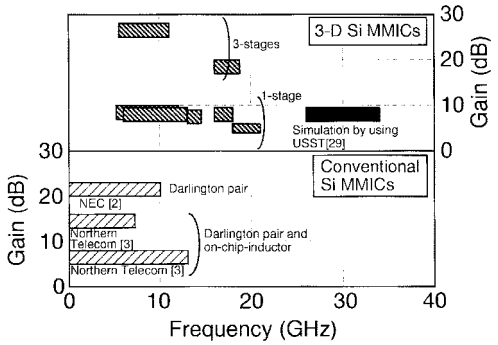
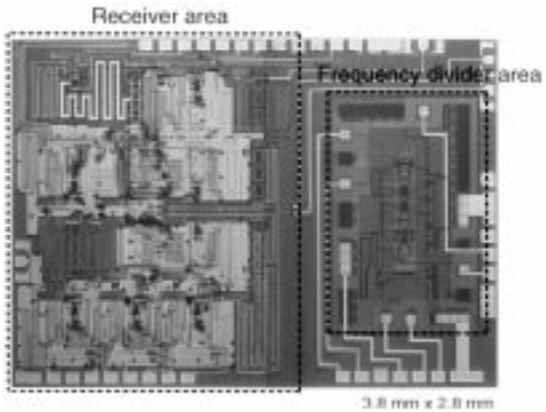


Fig. 13. Operation frequency comparison between 3-D Si MMIC amplifiers and Darlington-pair-based conventional Si MMIC amplifiers.



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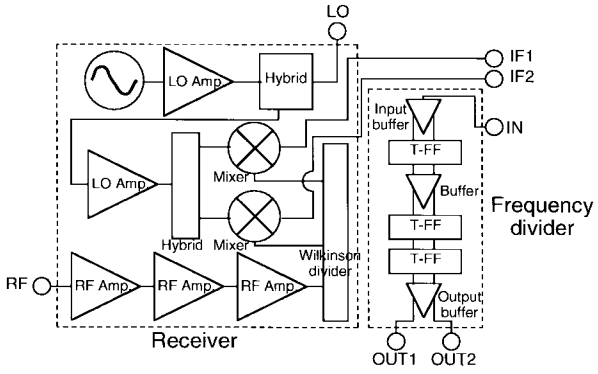

(b)

Fig. 14. Microphotograph of 3-D highly integrated mixed-mode Si MMIC chip. This chip comprises a receiver and a 1/8 frequency divider in an area of 3.8 mm $\times$ 2.8 mm.

by using high-performance Si bipolar transistor with an $f_{\max}$ of more than 70 GHz [29]. These results indicate that 3-D Si MMIC amplifiers can operate in the K-band frequency range with the use of standard Si bipolar transistors and have the potential to operate in the millimeter-wave frequency range by using recently developed high-performance Si devices.

B. Application to Highly Integrated ICs

The above results prove that 3-D Si MMIC's can operate in the K-band frequency range even if they use the same transistors as used in digital IC's. Fig. 14 shows a microphotograph

of a highly integrated mixed-mode IC for demonstration. This chip comprises a receiver and a 1/8 frequency divider in a chip size of 3.8 mm $\times$ 2.8 mm. The receiver comprises a three-stage RF amplifier, an LO amplifier and an image-rejection mixer constructed with two mixers, a Wilkinson divider and a multilayer broadside coupler, a voltage-control oscillator with an LO amplifier, and a hybrid for LO signal branch. The frequency divider is designed with an input buffer, three toggle flip-flops (T-FF's), and an output buffer. The master array and the core circuit of the frequency divider are fabricated by the Si IC process. The receiver and port connections of the frequency divider are fabricated by the 3-D MMIC process. This example shows that the 3-D Si MMIC process can effectively combine analog and digital IC's in a MMIC chip. In addition, this technology has the potential for allowing the application-specific integration circuit (ASIC) design method to be applied to MMIC's.

V. Conclusion

3-D Si masterslice MMIC technology allows Si MMIC's to achieve K-band operation, and the performance levels of the resulting 3-D Si MMIC's are competitive with those of GaAs MESFET MMIC's. X- and K-band mixers and amplifiers were demonstrated. The 3-D Si MMIC's have the potential to operate in the millimeter-wave frequency range if high-performance Si devices are used. In addition, this technology is extremely effective for analog–digital mixed IC's up to the K-band.

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